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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/588,508	06/06/2000	Guy Lynn Guthrie	AT9-99-505	8141

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BRACEWELL & PATTERSON LLP
PO BOX 969
AUSTIN, TX 78767-0969

EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/588,508	GUTHRIE ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2000 and 30 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-11 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Revocation Power of Attorney and Address change as received on 30 July 2002.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 5-6, and 9 are rejected under 35 U.S.C. 102(e) as being taught by Morris et al., U.S. Patent Number 6,079,012 (herein referred to as Morris).

6. Referring to claim 1, Morris has taught a data processing system comprising:

a. An interconnect (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; column 8, lines 1-12 and 52-58; Figure 9; and Figure 10);

b. A processor that processes memory access requests in program order (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; column 8, lines 1-12 and 52-58; Figure 9; and Figure 10);

c. A memory system coupled to said processor which supports memory access requests in a weakly consistent order (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; column 8, lines 1-12 and 52-58; Figure 9; and Figure 10); and

d. A controller that issues said memory access requests to said memory system and places a barrier operation on said interconnect in response to each memory access request issued (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; columns 6-7, lines 60-67; columns 8-9, lines 1-18; and Figures 8-10). In regards to Morris, the control signal prevents more instructions from executing, similar to a barrier operation.

7. Referring to claims 2 and 6, Morris has taught wherein said controller includes means for creating said barrier operations (Morris Abstract; columns 3-4, lines 65-27; columns 6-7, lines 60-67; columns 8-9, lines 1-18; and Figure 8).

8. Referring to claim 5, Morris has taught a processor comprising:

a. An instruction sequencing unit (ISU) that receives memory access instructions in program order (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; columns 6-7, lines 60-67; columns 8-9, lines 1-18; and Figures 8-10);

b. A load store unit (LSU) including a controller that issues memory access requests associated with said memory access instructions to an interconnect and places a

barrier operation on said interconnect in response to each memory access request issued (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; columns 6-7, lines 60-67; columns 8-9, lines 1-18; and Figures 8-10).

9. Referring to claim 9, Morris has taught a method of processing instructions in a data processing system, said method comprising the steps of:

a. Receiving an instruction sequence at a processor in program order, said instruction sequence including a memory access instruction (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; column 8, lines 1-12 and 52-58; Figure 9; and Figure 10);

b. In response to receipt of said memory access instruction, creating a memory access request and a barrier operation (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; columns 6-7, lines 60-67; columns 8-9, lines 1-18; and Figures 8-10);

c. Placing said barrier operation on an interconnect after said memory access request is issued to a memory system (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; columns 6-7, lines 60-67; columns 8-9, lines 1-18; and Figures 8-10); and

d. Upon completion of said barrier operation, completing said memory access request in program order (Morris Abstract; column 1, lines 15-21; columns 3-4, lines 65-27; columns 6-7, lines 60-67; columns 8-9, lines 1-18; and Figures 8-10).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 3-4, 7-8, and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al., U.S. Patent Number 6,079,012 (herein referred to as Morris) as applied to claims 1, 5, and 9 above, in view of Karp et al., U.S. Patent Number 6,321,328 (herein referred to as Karp).

12. Referring to claims 3-4, 7-8, and 10-11, Morris has not explicitly taught

a. Wherein said controller includes means for speculatively issuing load requests to said memory system while a barrier operation is pending (Applicant's claims 3 and 7).

b. Wherein said controller includes means for allowing data returned by a speculatively issued load request to be utilized by said processor only when an acknowledgment is received from all barrier operations pending when said load was issued (Applicant's claims 4 and 8).

c. Wherein said memory access request is a load request and further including the step of speculatively issuing said load request while a barrier operation is pending (Applicant's claim 10)

d. The step of forwarding data returned by said speculatively issued load request to a register or execution unit of said processor, when an acknowledgment is received for said barrier operation (Applicant's claim 11).

13. However, Morris has taught executing some instructions out-of-order to improve processor performance (Morris column 1, lines 22-37 and columns 3-4, lines 65-27). Karp has explicitly taught:

a. Wherein said controller includes means for speculatively issuing load requests to said memory system while a barrier operation is pending (Applicant's claims 3 and 7) (Karp Abstract; column 1, lines 1-20 and 41-47; and columns 1-2, lines 66-18).

b. Wherein said controller includes means for allowing data returned by a speculatively issued load request to be utilized by said processor only when an acknowledgment is received from all barrier operations pending when said load was issued (Applicant's claims 4 and 8) (Karp Abstract; column 1, lines 1-20 and 41-47; and columns 1-2, lines 66-18).

c. Wherein said memory access request is a load request and further including the step of speculatively issuing said load request while a barrier operation is pending (Applicant's claim 10) (Karp Abstract; column 1, lines 12-20 and 41-47; and columns 1-2, lines 66-18).

d. The step of forwarding data returned by said speculatively issued load request to a register or execution unit of said processor, when an acknowledgment is received for said barrier operation (Applicant's claim 11) (Karp Abstract; column 1, lines 12-20 and 41-47; and columns 1-2, lines 66-18).

14. It is known in the art and taught in Morris that executing instructions out-of-order is a common technique to improve processor efficiency. Karp has also taught out-of-order execution

improves processor efficiency by improving memory latency. However, barrier operations decrease the efficiency of processor, since they prevent instructions from executing until the current batch has completed, ensuring program order. Karp has taught speculative issuing of load instructions also improves processor efficiency by improving memory latency and ensures that data that is currently needed for execution is not displaced (Karp column 1, lines 41-60 and columns 1-2, lines 66-18). It would have been obvious to speculatively issue load instruction, as taught by Karp, because speculative loads increase a processor's efficiency by decreasing memory latency associated with fetching data from memory (Karp column 1, lines 11-20). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the speculatively issued load instruction of Karp in the device of Morris to decrease memory latency and increase processor speed.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Heidelberger et al., U.S. Patent Number 5,611,070, has taught a write/load cache protocol for maintaining cache coherency and performing barrier synchronization.

b. Gupta et al., U.S. Patent Number 5,802,374, has taught barrier synchronization.

c. Sproull, U.S. Patent Number 6,038,646, has taught barrier instructions with regards to a system with read and write paths.

d. Morris et al., U.S. Patent Number 6,286,095, has taught a system that ensures load and store operations execute in program order.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

18. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

May 5, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100